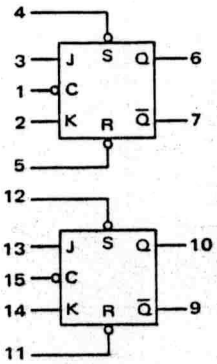
ML688T
Dual J-K Flip-Flop

Legacy Device: *Motorola MC688T*

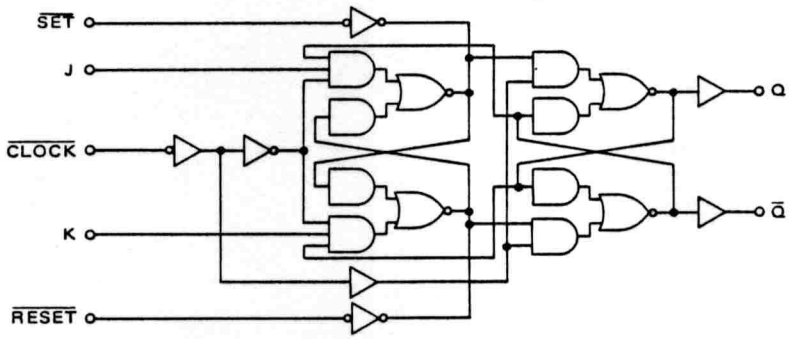


V_{CC} = Pin 16
Gnd = Pin 8

The negative–edge–clocked dual J-K flip-flop operates on the master–slave principle. His device provides both SET and RESET inputs on both flip-flops in the package. Each flip-flop may be set or reset by applying a low level to that particular input when the clock is low.

The J and K inputs are inhibited when the clock is low and enabled when the clock is high. The logical state of the J and K inputs MUST NOT be allowed to change when the clock is in the high state.

LOGIC DIAGRAM
1/2 OF DEVICE SHOWN



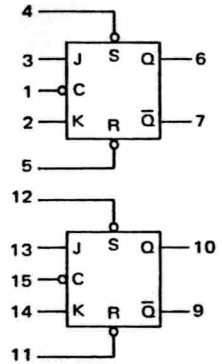
TRUTH TABLE

	R	S	t_n J	t_n K	t_{n+1} Q	t_{n+1} Q̄
•	0	1	x	x	0	1
•	1	0	x	x	1	0
	1	1	0	0	Q_n	$\bar{Q}_n$
	1	1	0	1	0	1
	1	1	1	0	1	0
	1	1	1	1	Q_n	$\bar{Q}_n$

0 = Low state
1 = High state
x = Don't care
t_n = Time period prior to negative transition of clock pulse.
t_{n+1} = Time period subsequent to negative transition of clock pulse.
Q_n = State of Q output in time period t_n.
• = Clock pulse must be in low state

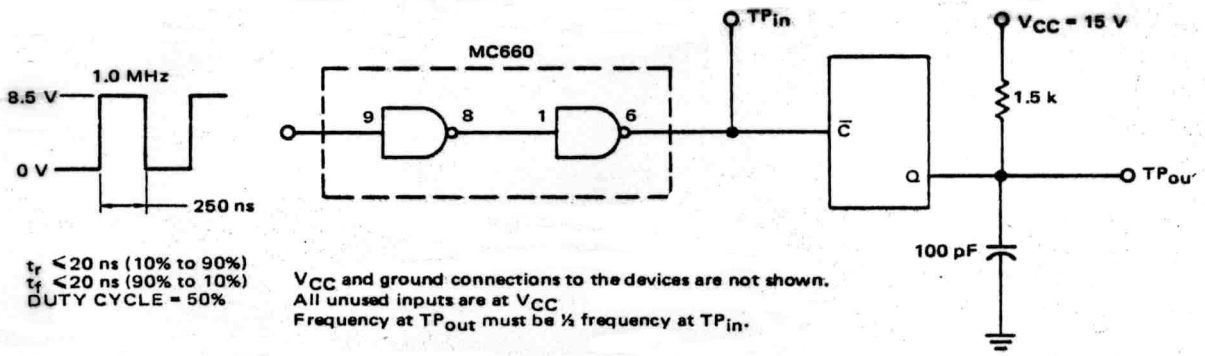
ELECTRICAL CHARACTERISTICS

Unless otherwise noted, tests are shown for only one flip-flop. The other flip-flop is tested in the same manner.



Characteristic	Symbol	Pin Under Test	688 Test Limits -30°C Min	-30°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	Unit	TEST CURRENT/VOLTAGE VALUES (All Temperatures) mA I_{OL}	mA I_{OH}	Volts V_{IL}	Volts V_{IH}	Volts V_F	Volts V_R	Volts V_{CCL}	Volts V_{CCH}	Volts V_{CC}	Volts V_{CEX}	CP_a	Gnd
										12.0	-0.03	6.50	8.50	1.5	16.0	14.0	16.0	15.0	16.0		
										TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW:											
Output Voltage	V_{OL}	6	–	1.5	–	1.5	–	1.5	Vdc	6	–	1,5	2,3,4	–	–	16	–	–	–	–	8
		7	–	↓	–	↓	–	↓	↓	7	–	1,4	2,3,5	–	–	↓	–	–	–	–	↓
		6	–		–		–			6	–	3	2,4,5	–	–		–	–	–	1	
		7	–		–		–			7	–	2	3,4,5	–	–		–	–	–	1	
	V_{OH}	6	12.5	–	12.5	–	12.5	–	Vdc	–	6	1,4	2,3,5	–	–	16	–	–	–	–	8
		7	↓	–	↓	–	↓	–	↓	–	7	1,5	2,3,4	–	–	↓	–	–	–	–	↓
		6		–		–		–		–	6	2	3,4,5	–	–		–	–	–	1	
		7		–		–		–		–	7	3	2,4,5	–	–		–	–	–	1	
Leakage Current	I_{CEX}	6	–	–	–	100	–	100	µAdc	–	–	–	–	–	–	–	–	2,3,5	6,16	–	1,4,8
		7	–	–	–	100	–	100	µAdc	–	–	–	–	–	–	–	–	2,3,5	7,16	–	1,5,8
Short Circuit Current	I_{SC}	6	-6.5	-15	-6.5	-15	-6.5	-15	mAdc	–	–	–	–	–	–	16	–	2,3,5	–	–	1,4,8,6
		7	-6.5	-15	-6.5	-15	-6.5	-15	mAdc	–	–	–	–	–	–	16	–	2,3,4	–	–	1,5,7,8
Reverse Current	I_R	1	–	–	–	2.0	–	2.0	µAdc	–	–	–	–	–	1	16	–	–	–	–	8
		2	–	–	–	↓	–	↓	↓	–	–	–	–	–	2	↓	–	–	–	–	1,8
		3	–	–	–		–			–	–	–	–	–	3		–	–	–	–	1,8
		4	–	–	–		–			–	–	–	–	–	4		–	–	–	–	8
		5	–	–	–		–			–	–	–	–	–	5		–	–	–	–	8
Forward Current	I_F	1	–	-1.20	–	-1.20	–	-1.20	mAdc	–	–	–	–	1	–	–	16	–	–	–	8
		2	–	-1.20	–	-1.20	–	-1.20	↓	–	–	–	–	2	–	–	1,16	–	–	–	4,8
		3	–	-1.20	–	-1.20	–	-1.20		–	–	–	–	3	–	–	1,16	–	–	–	5,8
	$2I_F$	4	–	-2.4	–	-2.4	–	-2.4		–	–	–	–	4	–	–	16	–	–	–	1,2,3,5
		5	–	-2.4	–	-2.4	–	-2.4	↓	–	–	–	–	5	–	–	16	–	–	–	1,2,3,4
Power Drain Current (Both Flip-Flops)	I_{CCL}	16	–	–	–	35	–	–	mAdc	–	–	–	–	–	–	–	16	–	–	–	1,2,3,4,5,8,11 12,13,14,15
	I_{CCH}	16	–	–	–	30	–	–	mAdc	–	–	–	–	–	–	–	16	–	–	–	8

Pins not listed are left open.



SWITCHING CHARACTERISTICS

Characteristic	Symbol	-30°C	25°C		+75°C	Units
		Typ	Min	Typ	Typ	
Propagation Delay						
Delay from $\overline{S}$ to $\overline{Q}$	t_{pd-}	65	–	80	100	ns
Delay from $\overline{R}$ to $\overline{Q}$	t_{pd-}	65	–	80	100	ns
Delay from $\overline{S}$ to Q	t_{pd+}	250	–	300	400	ns
Delay from $\overline{R}$ to $\overline{Q}$	t_{pd+}	250	–	300	400	ns
Delay from C to Q or $\overline{Q}$	t_{pd+}	300	–	350	450	ns
Delay from C to Q or $\overline{Q}$	t_{pd-}	85	–	100	130	ns
J or K Input	t_{setup}	55	–	60	70	ns
J or K Input	t_{hold}	26	–	24	0	ns
f_{Toggle}	f_{Tog}	–	1.0	2.5	–	MHz

OPERATING NOTES

1. If any of the input of ML688 is not used, it should be returned through a 2kΩ resistor to VCC. This is particularly true of the $\overline{SET}$ and $\overline{RESET}$ inputs, as these are most susceptible to noise. A single resistor may be used for up to 300 unused inputs.
2. The truth table shown for ML688 is completely valid only when the J & K inputs remain unchanged throughout the entire period when the clock input is high. This is a master-slave device, with the master receiving its instructions while the clock input is high. A study of the logic diagram will reveal that the J & K inputs are such that the flip-flop should reverse states at the negative clock transition, it will reverse state on the negative clock transition regardless of any subsequent change of J or K.

   The master-slave principle as used in this device leads to the aforementioned restriction which may not be desir able in some instances. However, it can be shown that an MHTL system is inherently more susceptible to negative-going nose than positive-going due to the difference in impedance levels.The design of the ML688 is such that negative-going noise appearing on the J or K inputs must last throughout the entire duration of the clock pulse to have any effect. The net result can well be a system with greater than expected noise immunity if care is used in other areas of the system.
3. The $\overline{SET}$ and $\overline{RESET}$ inputs control the output states when activated while the clock is low. A logic zero on these inputs has no immediate effect on the outputs if the clock input is high, but it can change the state of the master section. As an example, consider $\overline{SET}$ & $\overline{RESET}$ high, all other inputs and Q output low. If a clock pulse is received under these conditions, the output will not change. However, if $\overline{SET}$ is momentarily activated with a logic zero while clock is high, the flip-flop will reverse states on the trailing edge of the clock. This provides a means of syn chronous data entry into the devices without using J & K inputs. This feature is quite useful in certain types of shift registers and counters made with the ML688.
4. As with other saturated logic devices, input rise and fall times should be minimized for best operation. The most critical input in this respect is $\overline{CLOCK}$, which should have a transition time of less than 0.5 □ sec in either direction (measured from 6.5 to 8.5 volts). Failure to observe this restriction may result in triggering on positive clock transition or multiple triggering on negative clock transition.